Integrating MOSFETs And Drive Circuitry For Power Supply Applications

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MOSFETs packaged with driver products are gaining in popularity among power supply designers. The advantage of co-packaging the MOSFET pair with the driver is three-fold. Elimination of the drivers from the PWM controller allows for a smaller controller IC for lower cost, and a reduction of the heat generated: For better stability of the reference voltage. Combining the driver with the MOSFET pair eliminates PCB parasitic components and allows for a reduction in gate drive losses and higher operating frequency. Lastly, there is a reduction of PCB real estate by going from a driver with 2 MOSFETs for a count of three SO-8 packages (90 mm²), to a single SO-16 (60mm².)

Four of the key characteristics of this type of product are optimized MOSFET and driver, optimized cross-conduction losses, and "shoot-thru" ruggedness.

The specifics of how a MOSFET is optimized depend on its duty cycle as a high-side switch. For a notebook core application, with an 18-V input and a 1.5-V typical output, the duty cycle can be less than 10%. For desktop applications with a 12-V input and 1.5-V output, the duty cycle can be around 13%. For point-of-load (POL) converters the duty cycle can be 30% to 50% depending on the voltage requirements. In low-duty-cycle applications the size of the high-side MOSFET is usually smaller than the low-side MOSFET to minimize switching losses and the low-side MOSFET size is optimized to minimize conduction losses.

An analysis of how efficiency varies with the change in die-size ratio between high-side and low-side MOSFET area was performed for a given process technology and MOSFET cell density. Desktop applications achieve the best performance with a 0.5:1.0 die-size ratio. As the die-size ratio increases switching losses become dominant and progressively reduce efficiency. As the die-size ratio decreases conduction losses tend to drive the efficiency lower. For lower-duty-cycle applications, such as notebook core applications, the optimal die-size ratio is 0.3:1.0. For higher-duty-cycle applications, such as POL converters, the ideal die-size ratio is 0.8:1.0.

Driver optimization can have a significant effect on cross-conduction losses during the two transition periods of the switching cycle: High-side turn-off to low-side turn-on and low-side turn-off to high-side turn-on (dead-time.) The first event is typically controlled through adaptive switching which ensures that the high-side MOSFET is turned off before the low-side is turned on. The second transition is usually a fixed time and when this time is long, say 50 ns, it is possible that the low-side body diode will conduct and thereby reduce the efficiency of the circuit. Whereas, when the dead-time is too short there can be excessive cross-conduction losses. Optimized dead-time can minimize the body diode conduction and allow some cross-conduction. This can effectively reduce the peak ringing voltage on the high-side MOSFET and there will be less stress on the

MOSFET, allowing designers to use a lower V_{DS}-rated MOSFET for improved performance or reduced cost.

Silicon Technology Advancement

One silicon optimization method is to use a MOSFET with a lower gate threshold, V_{th}. This has three effects on the MOSFET:

Event	Issue	Parameters	Effects
Turn-off	Ringing	$t_f = R_G C_{iss} / V_{th}$	Allows longer turn-off time
Turn-on	Body diode	$t_r = R_G C_{iss} / (V_{GS}-V_{th})$	Reduces rise time
Conduction	Low $R_{DS(on)}$	$R_{DS} \sim 1 / (V_{GS}-V_{th})$	Lower R

Table 1: Effects Of Low V_{th}

For the turn-off period a lower V_{th} slows down the turn-off and also allows some cross-conduction to help dampen any ringing that is the result of the high-side turning on. A lower threshold helps in turning on the low-side MOSFET by reducing the rise time. The third effect of the lower threshold is the reduction of conduction losses due to lower $R_{DS(on)}$. The last two are more applicable with a 5-V gate drive than with higher gate-drive voltages.

The second silicon optimization that is required is that of shoot-thru ruggedness. Shoot-thru occurs when the high-side turns on, causing a high dV/dt transition of the switching node. The sharp voltage rise can inflict a voltage pulse on the low-side MOSFET gate due to the Miller capacitance. When lowering the gate threshold this condition is more of a concern. However, proper selection of MOSFET parameters and optimization of the MOSFET process can help reduce this effect. With control over the ratio of the Miller capacitances, C_{gd} and C_{gs}, the V_{GS} pulse may be limited by the equation:

$$V_{GS}(t_0) = R_G * C_{rss} * \frac{V_{DS}}{t_o}\left(1 - e^{\frac{-t_0}{R_G * C_{iss}}}\right)$$

If $R_G = 2\ \Omega$, $V_{DS} = 12$ V, and rise time t_o=20 ns, then for a set condition, a family of curves can be generated. For a C_{iss}=4 nF, the C_{rss}/C_{iss} ratio needs to be less than 0.4 (Q_{gd}/Q_{gs} ratio of 1.0) for a typical threshold of 1.8 V to 2 V. Use of a low-threshold MOSFET requires a ratio of less than 0.25 (Q_{gd}/Q_{gs} ratio of 0.8) to ensure that shoot-thru is minimized.

Products integrating power MOSFETs and driver circuitry work well with low-cost controllers that lack output driver stages and in designs where the PWM controller is integrated onto an ASIC. Devices with breakdown voltages of 30 V are suited for applications such as notebook computers, while 20-V products are useful for desktop applications and POL converters and allow for better MOSFET parameters such as lower

$R_{DS(on)}$ and smaller switching losses. Currently, such devices are available in packages as small as the SO-16.

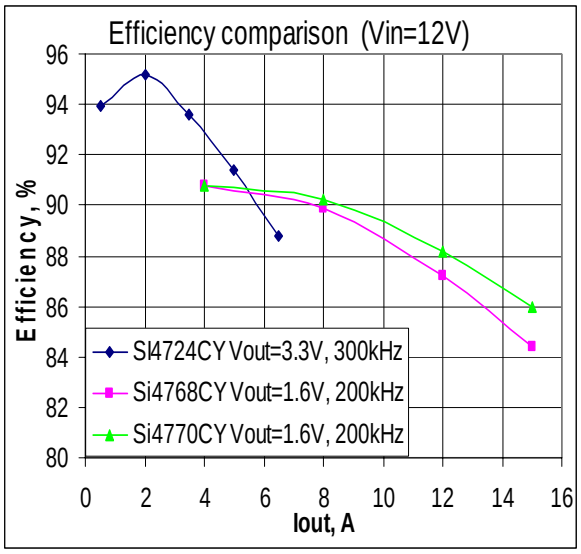

Fig. 1: SO-16 Product Efficiency

Through optimization of die size, dead-time control, and silicon optimization, efficiencies above 84% are possible. In Fig. 1 30-V products show results vs. application current. SO-16 product efficiencies tend to limit around 15 A for 200 kHz when used for computer-related applications such as DDR, auxiliary, and multi-phase VRM power supplies.

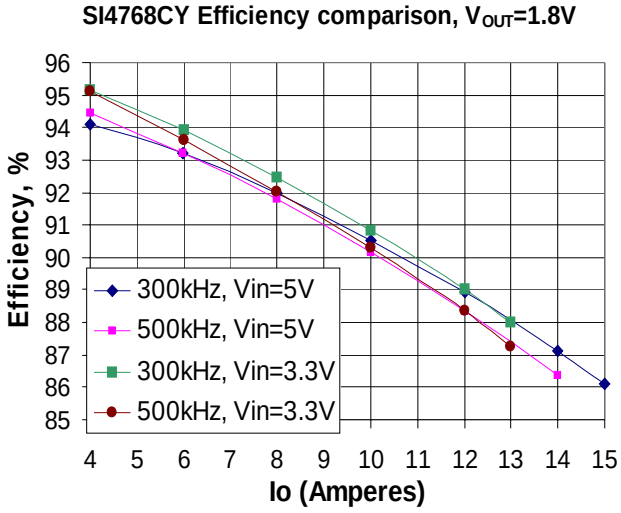

Fig. 2: POL Efficiency Results, Two-Phase Board

The SO-16 products were also tested in POL applications. Because POL converters require less current the SO-16 package is very appealing in cost and performance. Fig. 2 shows the efficiency results for a set of POL conditions, where efficiencies are above 86% for the SO-16 package (Si4768CY) with loads up to 14 A at 500 kHz.

Conclusions

Integrated MOSFET and driver products can provide performance improvements for computer core voltage regulators and for other dc-to-dc synchronous-buck power supplies. MOSFET-plus-driver integrated devices offer excellent efficiency for applications up to 15 A. Built on optimization of the die-size ratio, dead-time control, and MOSFET and driver optimization, an integrated device packaged in the SO-16 can reduce board space requirements by as much as 60% while delivering equivalent performance to four discrete MOSFETs plus driver circuitry.

About The Author

Derek Koonce works in Market Development and Applications for the power MOS product group at Vishay Siliconix focusing on the computer and communication segments, including PCs, digital cameras, printers, PDAs, cell phones and fixed power supplies. Prior to 2000 Mr. Koonce was Senior Applications Engineer at Supertex specializing on high-voltage ICs for flat panel displays, high-speed printers, and power supplies. His experience also includes 7½ years as a development engineer for Loral Electro-Optical Systems in the field of power supplies, flash lamp drivers, CCDs, and analog instrumentation. He earned a BSEE from California State University at Northridge.