Optimizing P-Channel Power MOSFETs for DC/DC Conversion

By Derek Koonce and Deva Pattanayak

Vishay Siliconix
2201 Laurelwood Road, MS 70
Santa Clara, CA 95054
1 408 567-8948
derek.koonce@vishay.com
deva.@pattanayak@vishay.com

Abstract

Low-power wireless electronics where the output power is less than 10 W represent one of today's biggest dc-to-dc converter design challenges. Size must be kept to a minimum while maintaining an acceptable level of efficiency.

One common way to reduce converter size is to specify a higher operating frequency. Faster switching means a smaller inductor can be used. Schottky diodes are sometimes used for synchronous rectification in these circuits, but MOSFETs are a better choice as output voltages decrease, since the voltage drop can be significantly less than the diode.

An additional space-saving technique is to replace the n-channel synchronous MOSFET with a p-channel device. The p-channel approach eliminates the need for additional circuitry to drive the gate, as required when an n-channel is used on the high side. But until now, p-channel MOSFETs have been optimized for load switching applications, with switching speeds that are too slow for dc-to-dc converter applications.

A new type of p-channel MOSFET optimized for low switching losses at high frequencies removes this trade-off while eliminating secondary turn-on effects, giving designers the space-saving benefits of the p-channel solution while maintaining a high level of converter efficiency. This paper will address the optimization process used to develop an optimized p-channel MOSFET, and will present test results showing its performance improvement compared with p-channel MOSFETs optimized for load switching.

Using P-Channels for Switching and Rectification

There are several dc-to-dc applications that can benefit from the use of p-channel MOSFETs. In either a synchronous buck or an asynchronous buck converter, a p-channel MOSFET can be used to switch on the high-side voltage and charge the output inductor (Figure 1a). In a boost converter (Figure 1b) the p-channel MOSFET is used as the output rectifier. In such <1.8-V input voltage applications, the body diode is used during start-up to build up the output voltage. Once the output voltage has increased above 1.8 V, the p-channel MOSFET can provide a lower voltage drop and hence a more efficient circuit than a rectifying diode implementation. A p-channel implementation of a voltage inverter is shown in Figure 1c. As in the buck converter example, the p-channel MOSFET is used to charge the inductor by turning on the input voltage to the circuit.

In all three of these applications, the key parameters guiding MOSFET selection are device on-resistance, $r_{(DS)on}$ and gate charge, Q_g. Since neither parameter by itself is sufficient to predict device performance in a dc-to-dc circuit, designers use the product of $r_{DS(on)}$ and Q_g as the figure of merit for selecting MOSFETs to be used in this application. This figure of merit becomes more important as the frequency of the converter increases, since switching losses can exceed conduction losses. Maintaining a low Q_{gd}/Q_{gs} ratio is also important to prevent the p-channel MOSFET from turning on again when the drain voltage is pulled to ground.

Beyond Load Switching for P-Channel MOSFETs

P-channel MOSFETs are most often used for load switching. The simplicity of p-channel solutions makes them equally attractive for dc-to-dc converters in portable electronics systems where space is at a premium. Until now, however, p-channel devices optimized for dc-to-dc conversion with low switching losses have not been available, and therefore designers have had to rely on n-channel MOSFETs requiring a larger number of components for a complete dc-to-dc solution.

Vishay Siliconix is addressing this trade-off with new p-channel power MOSFETs that have been optimized for dc-to-dc switching performance in the same manner as its successful PWM-optimized n-channel devices. The new PWM-optimized p-channel MOSFETs devices are built on a 113 million-cells per square inch Trench technology that delivers an impressive improvement in switching loss performance. Table 1 compares specifications for p-channel MOSFETs optimized for load switching with devices optimized for dc-to-dc conversion. Each device listed in the table is offered in the LITTLE FOOT TSOP-6 and uses the maximum silicon area possible in this package type.

Trench power MOSFETs, the preferred device type for applications where on-resistance must be kept at ultra-low levels, are currently fabricated in two forms: closed-cell and stripe. In the closed-cell version, each transistor cell is a four-walled structure, whereas in the stripe version, each transistor cell has only two walls. On-resistance decreases with cell density, which refers to how many such cells can be placed in a square millimeter. Each of the cells is a vertical transistor, and these are all tied in parallel to produce the overall device MOSFET.

In Figure (2) and (3) we compare the topologies of a 2.7-micron pitch closed-cell and stripe cells. The red regions denote the trench in which the gate Poly Silicon is deposited. A comparison of Figures 2 and 3 clearly shows that for the same cell area, gate width is higher in the closed-cell (four-walled) MOSFET topology than in the stripe cell (two-walled) topology. In the closed-cell Trench MOSFET, the $r_{DS(on)}$ of the device is kept low since there are four walls to provide the resistance path. However, this trench wall area also contributes to the gate charge of the MOSFET. In the stripe topology (Figure 3), two of the closed cell walls have been knocked out to form a long trench. The $r_{DS(on)}$ is increased, but the gate charge has been reduced since there is not as much wall area as before. The overall result is a p-channel device with where the $r_{DS(on)}*Q_g$ figure of merit is improved and the Q_{gd}/Q_{gs} ratio is lowered.

Lowering the Q_{gd}/Q_{gs} Ratio

Figure 4 shows a trench MOSFET cross section. Q_{gs} is a function of the channel length of the MOSFET and the junction depth of the source, while Q_{gd} is a function of the overlap area of the PolySilicon gate with the drain region. To yield a lower Q_{gd}/Q_{gs} ratio, Vishay Siliconix focused on lowering Qgd by using a shallower trench while maintaining the same body depth.

In this process, the overlap of the PolySilicon gate with the p-drift region on the side of the trench is minimized. Caution must be used to keep a certain minimum side overlap of the PolySilicon gate with the drift region above the trench bottom, otherwise the drift region will be separated from the source through the inverted channel during the on-state of the MOSFET, resulting in excessive on resistance.

There are other ways of reducing Q_{gd}, such as narrowing the trench. For PWM-optimized p-channel MOSFETs, however, Siliconix chose to shallow the trench depth from 1.3 micron to 1 micron. This reduced the overall ratio of Q_{gd}/Q_{gs} to below 0.7, and this low ratio helps prevent any secondary turn on, or shoot through, condition in the p- channel striped-cell trench MOSFET.

Efficiency Test Results

Vishay Siliconix tested its new PWM-optimized p-channel technology with a Linear Technology LTC1773 evaluation board in a synchronous buck topology. The LTC1773 EVB was designed for a high-efficiency supply using minimal component count. The MOSFETs listed in Table 1 were used in the test. The power supply conditions for the results were V_{IN} = 8 V,V_{OUT} = 3.3 V, and I_{OUT} = 0.01 A to 2.0 A.

The Si3867DV shows the best efficiency results (Figure 5). A designer who wanted the lowest on-resistance possible might opt for the Si3491DV, but the trade-off is a 78% higher level of Q_g. As stated previously, for high frequency dc-to-dc applications, the key figure of merit is not $r_{DS(on)}$ by itself but $r_{(DS)on}$*Q_g, making the Si3867DV the best choice.

When comparing all the closed cell devices (Si3483DV, Si3443DV and Si3491DV) it is interesting to note that all yield similar values for the $r_{DS(on)}$*Q_g figure of merit. However, the Si3443DV shows the best efficiency even though it is not the lowest $r_{DS(on)}$. This can be explained by observing the gate waveform during the turn-off cycle.

Figure 6 shows the turn-off waveforms of the p-channel devices tested. In the Si3843DV and Si3491DV, devices built on a 90-million closed-cell p-channel process optimized for load switching, one can observe that the gate is pulled down sufficiently to turn on the MOSFET and cause a shoot-through, or secondary turn-on of the MOSFET. This can severely impact the efficiency of a dc-to-dc converter circuit—by as much as 12%. However, for the older-process (32-million closed-cell), Si3443DV and the new-process (113-million stripe-cell) Si3867DV, there is not a significant pull-down of the gate. Thus, the MOSFET is kept off.

Improvements to the silicon result in better efficiency and thus better thermal performance. In fact, MOSFET operating temperature can be reduced by as much as 10 °C thanks to improvements in efficiency. Figure 7 shows thermal images of the four devices operating at maximum output current. The temperature scale at the bottom of these pictures range from 25 °C for black to 65 °C for white.

Other Tests and Limitations

Output rectification

When a PWM-optimized p-channel power MOSFET is used for rectification in boost converters, its low $r_{(DS)on}$*Qg provides a lower power loss than a diode's V_f*I. With a Q_{gd}/Q_{gs} ratio less than 0.7, the secondary turn on of the MOSFET will also be minimized – an important point, since the MOSFET is in the reverse direction and the source of the device is connected to the output. When the n-channel MOSFET is turned on (figure 1b), the gate of the p-channel MOSFET can be pulled low due to the Miller capacitance.

Low frequency limitations

Additional dc-to-dc converter testing was performed using a lower switching frequency. It was found that at 100 kHz, the low-$r_{DS(on)}$ device [put in device number] delivered better efficiency, since the switching losses were no longer the major contributor to overall device losses. At this lower frequency, conduction losses predominate, so the low-$r_{DS(on)}$ device built on closed-cell technology is the better choice.

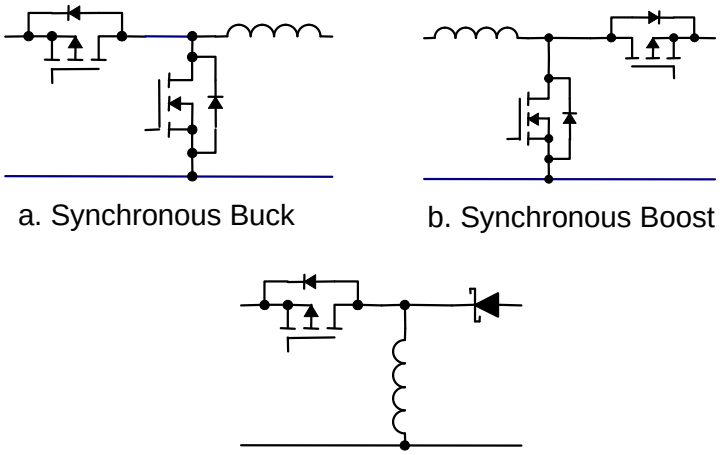
Conclusions

A new approach to dc-to-dc optimization for low-voltage power conversion has focused on optimizing the p-channel MOSFET technology. It has been shown that a stripe-trench technology can yield better efficiency and lower operating temperature when compared to the lower $r_{DS(on)}$ closed-cell technology. This optimization is particularly suited for converters operating at frequencies above 250 kHz. The new optimization not only focuses on the $r_{DS(on)}$*Qg figure of

merit, but also on the Q_{gd}/Q_{gs} ratio, which must be kept below 1 to minimize secondary shoot-through conditions as the MOSFET turns off.

Article Figures

Figures for PWM P- article / paper



a. Synchronous Buck

b. Synchronous Boost

c. Voltage Inverter

Figure 1. DC-DC topologies using P- channel MOSFETs

Table 0. P- channel specifications for TSOP-6 fill-the-paddle die

Name	V_{DS} (V)	V_{GS} (V)	$r_{DS(on)}$ 4.5	Q_g (nC) 4.5V	Q_{gs} (nC) Typ.	Q_{gd} (nC) Typ.	V_{th} V	Cell Density	$r_{(DS)on}*Q_g$	Q_{gd}/Q_{gs}
Si3483DV	-30	20	0.053	11	3.6	6	1	90M CC	0.58	1.67
Si3443DV	-20	12	0.065	8.5	2.8	1.7	0.6	32M CC	0.55	0.61
Si3491DV	-20	8	0.044	12.5	1.7	3.3	0.4	90M CC	0.55	1.94
Si3867DV	-20	12	0.051	7	2.3	1.6	0.6	113M St	0.36	0.7

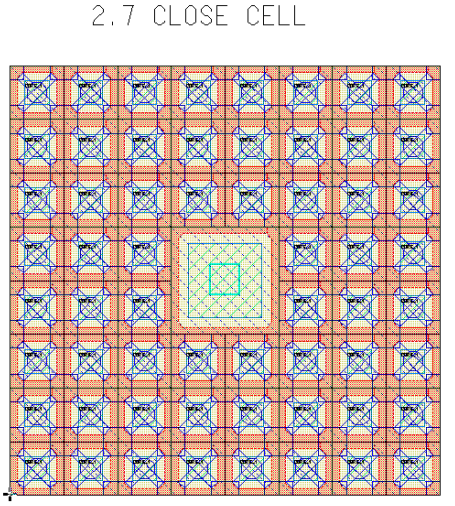


Figure 2. Closed Cell

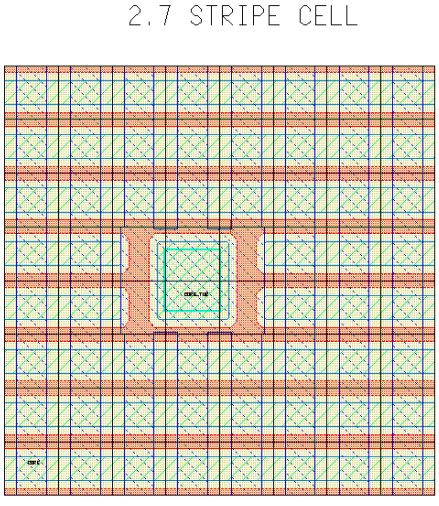


Figure 3. Stripe Cell

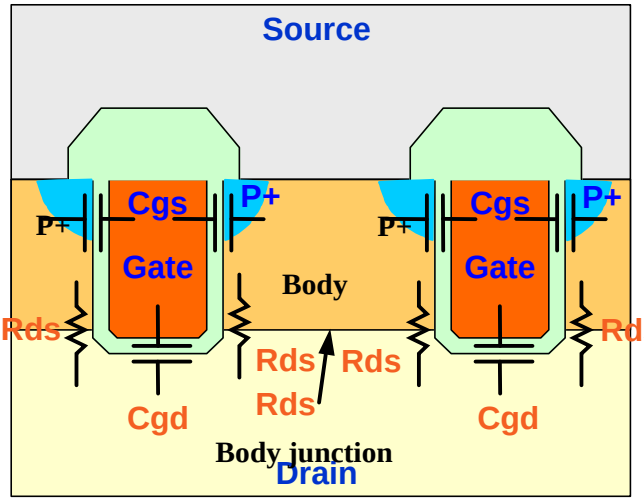


Figure 4. Cross section of Trench MOSFET

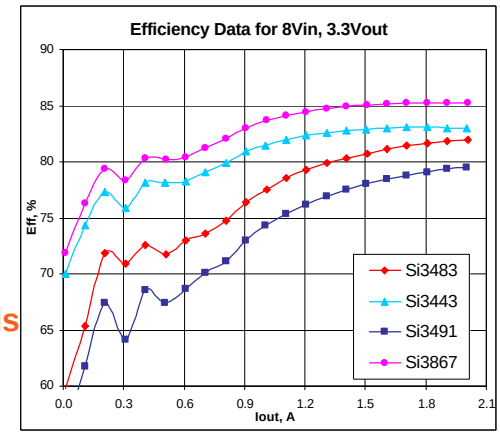


Figure 5. Efficiency results

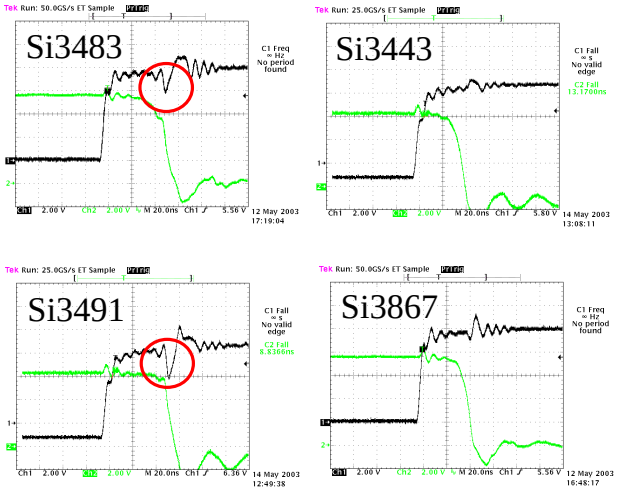


Figure 6. Turn off waveforms, Gate (black), Drain (green)

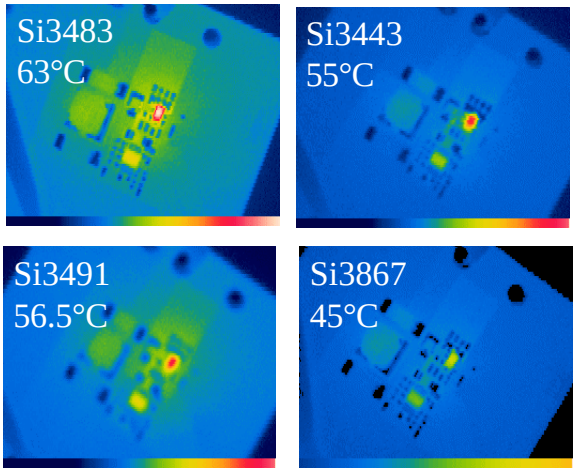


Figure 7. Thermal images at 2-A output