High Input Voltage, Low Wattage SMPS

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Introduction

Efficient high input voltage, low wattage switch mode power supplies, SMPS, are difficult to achieve. For example, a 20W SMPS with an efficiency of 90% may be impressive but it allows for 2.2W of losses. An SMPS with an efficiency of 60% at an output power of 25mW may not sound as impressive but is much more difficult to achieve. The total losses need to be less than 16.7mW. Every milliwatt of loss is crucial. Conventional pulse-width modulated (PWM) controllers can draw 17mA at 10V thereby consuming 170mW. This already exceeds the maximum power consumption by a factor of 10. The Supertex HV9605C PWM controller IC provides a solution for designers by minimizing power consumption.

Theory of Operation

A typical power supply employing the HV9605C can be described using six basic functional blocks as follows:

1. PWM control circuitry
   A. Start-up
   B. Power switch
   C. Current loop / current limit
2. Transformer
3. Output rectifier and filter
4. Feedback control loop
5. Start/stop control
6. Status output

The schematic in figure 1 will be referenced as each block is described.

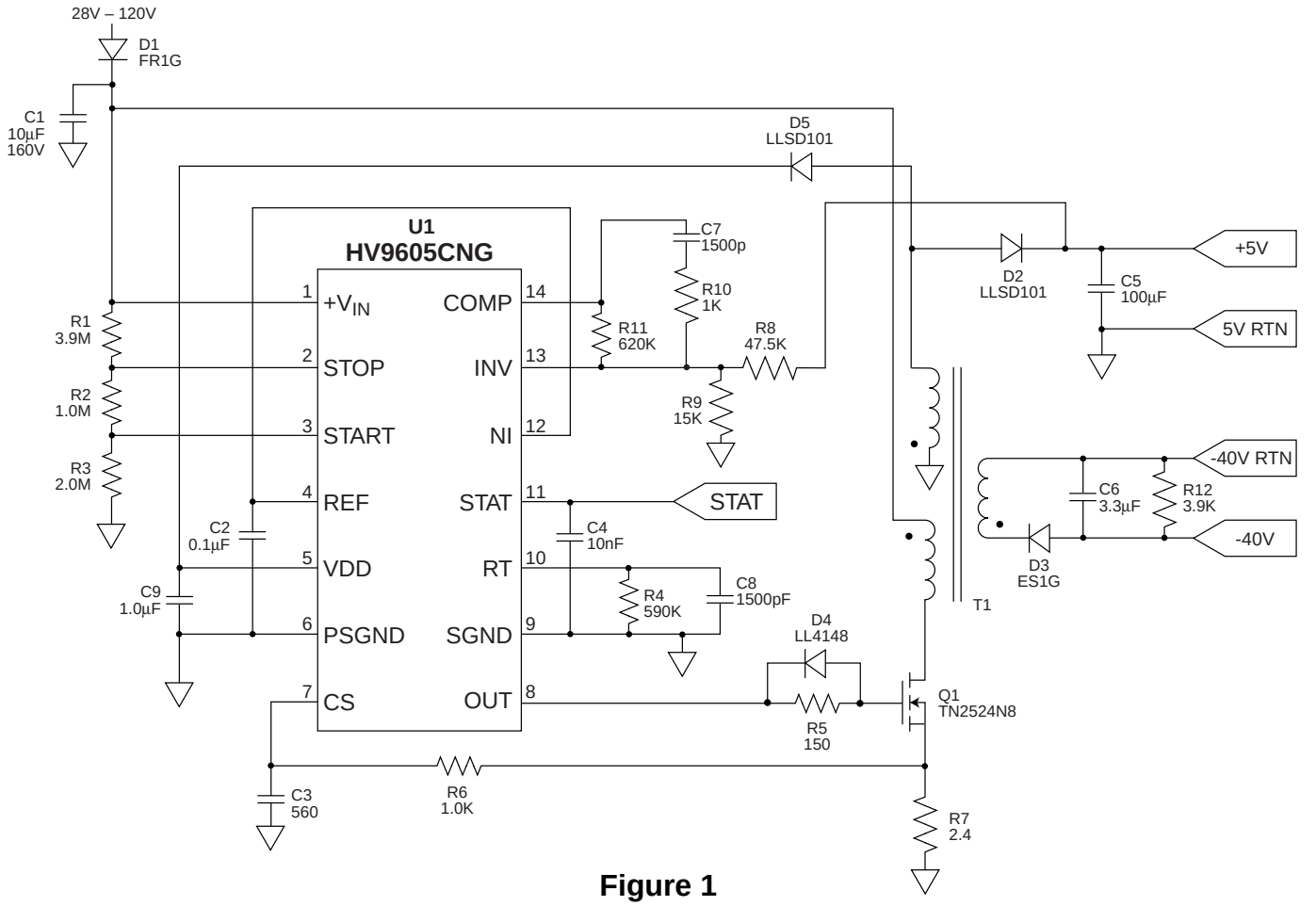

Figure 1

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PWM Control Circuitry

The HV9605C PWM IC, U_1, can be powered from a voltage source of up to 250 Volts. This ability comes from a state-of-the-art High Voltage BiCMOS process developed by Supertex. The capability to standoff high voltage can simplify the start-up circuitry required for the converter.

The HV9605C PWM IC is designed for applications requiring high efficiency at low output power, typically 1Watt. To minimize losses, the control circuitry is designed to operate at 5.0V. However, this limits the gate drive for the external MOSFET to 5.0V. Typical MOSFETs require 10V gate drive to fully turn on. Supertex low threshold MOSFETs are guaranteed to be fully on with only 5.0V gate drive making them ideal for this application.

Start-up

The only voltage available for any SMPS is the input voltage. If the input voltage is high, some means of generating a lower voltage to protect the PWM is required to start-up the controller. A conventional high voltage start-up circuit uses a resistor with a zener diode, figure 2. Once the PWM controller has started, an auxiliary winding is used to provide the operating current for the controller. The problem with this approach is that power is always being dissipated in the resistor. Using an input voltage of 48V as an example, typically 1.0mA will be drawn creating a constant power loss of 48mW for the start-up circuit.

The integrated high voltage start-up circuit of the HV9605C practically eliminates this loss.

The start up circuit for the HV9605C, detailed in figure 3, consists of a high voltage enhancement-mode MOSFET (M_1), an operational amplifier (A_1), and a voltage reference. When V_{IN} increases above the start threshold, typically 7.3V, the comparator, A_2, will turn on the reference voltage, oscillator and the internal regulator (M_1 and A_1). The amplifier A_1 is enabled and, in conjunction with M_1, generates a V_{DD} voltage. The V_{DD} powers the internal circuit and begins pulsing the gate of the power switch Q_1, turning it on and off.

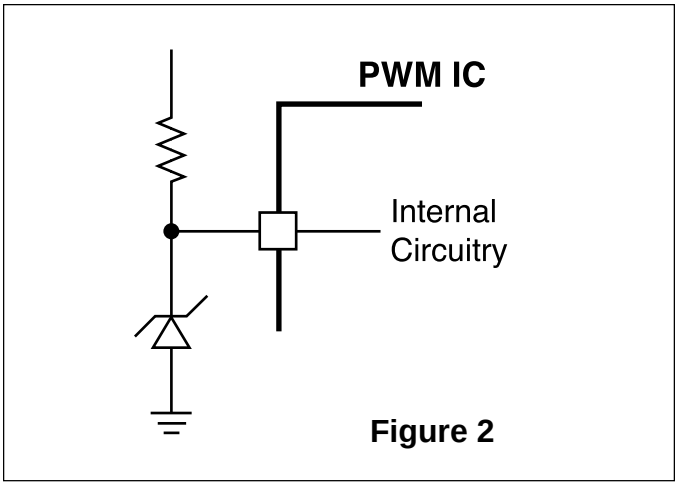

Figure 2

Referring to Figure 1, the primary winding of T_1 is charged when Q_1 is turned on. The energy stored in the primary is transferred to the secondary windings during the off state of Q_1. This charges capacitors C_5 and C_6. U_1's V_{DD} is generated from the 5V tap off the 5V secondary winding, storing energy to C_9. As the voltage across C_9 increases above 4.5V, the start-up circuit will automatically turn off. The V_{DD} supply for the HV9605C is now generated by the tap from the auxiliary winding. This also turns off M_1 and reduces the start up circuit power consumption to a negligible amount. The power loss in the start-up circuit is less than 1mW as compared to 48mW for the resistor zener diode approach.

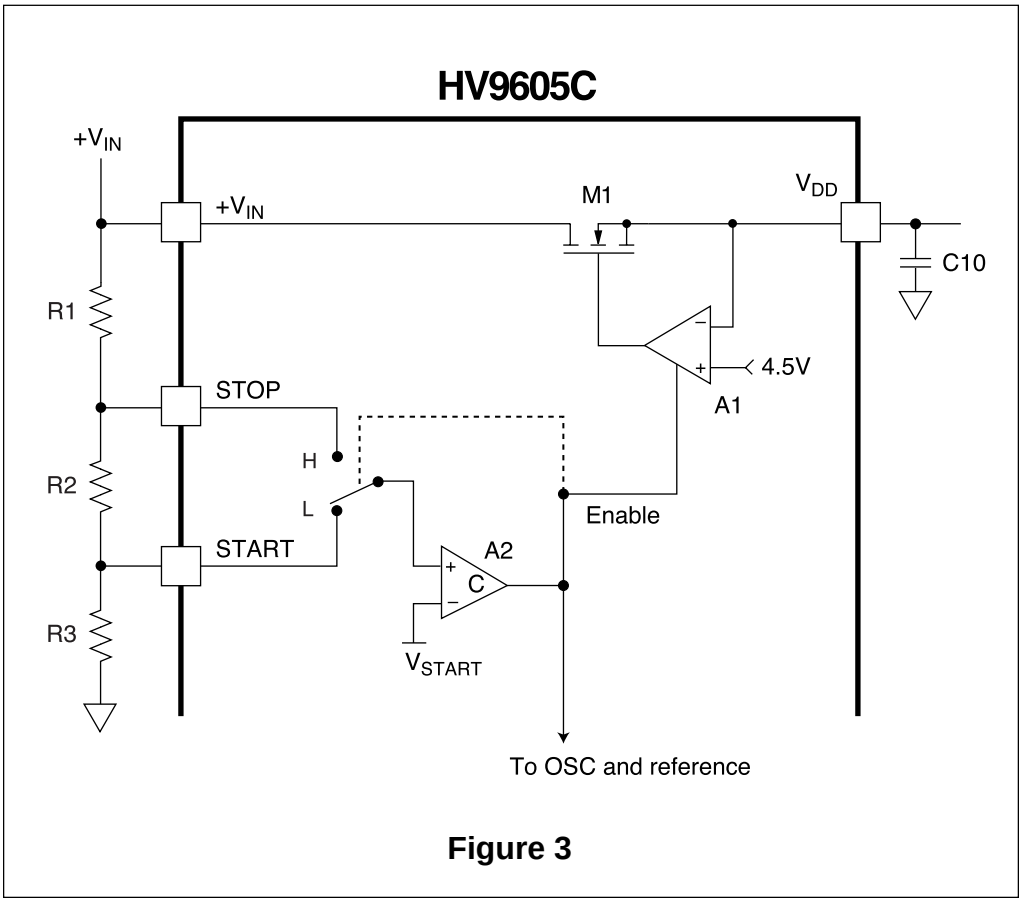

Figure 3

The operating I_{DD} current of the HV9605C is typically 0.9mA compared to a conventional PWM controller of 17mA. The typical operating power consumption for the HV9605C is only 5.0V x 0.9mA = 4.5mW as compared to a conventional PWM controller of 10V x 17mA = 170mW. By reducing both the operating voltage and current, power consumption is kept at a minimum.

Power Switch

The flyback cycle starts when the HV9605C MOSFET drive stage turns Q_1 on. This output drive stage has rail-to-rail swing for optimal drive of Q_1, the TN2524N8. This Supertex MOSFET is a low-threshold, 240V, 6Ω device designed to work in DC-DC converter applications like the HV9605C. Its low-threshold ensures that a 5V gate drive will provide ample gate biasing for low $R_{DS(ON)}$. In addition, the low input capacitance reduces the drive current required, thereby improving power converter

efficiency. Another feature is that the layout design engineer's task is easier by these lower currents because the parasitic elements in the gate path on the PC board become less critical.

Q_1 acts as a switch; it either conducts current (on), or does not conduct current (off). The time it takes for Q_1 to transition between the on state (conducting) and off state (not conducting) must be reduced to keep the power dissipation in Q_1 low and system efficiency high. The power dissipated in Q_1 comes from three primary sources:

1. Voltage and current across the device during the transition time between on and off states. In the discontinuous flyback design, there is little current in the off-to-on transition. Most of the losses occur during the on-to-off interval. We call these transition, or switching, losses.
2. When the switch is on, the current is building up in a linear ramp across the transformer primary winding. As this current increases, the dissipation in the switch also increases by the resistive loss: $I^2R_{DS(ON)}$ which is called the conduction loss. The TN2524N8 is available in small SOT-89 package to minimize board space and allow sufficient power dissipation. Reducing the $R_{DS(ON)}$ usually requires a larger MOSFET. This in turn would result in a larger gate capacitance, and slower turn-off times. The end result could mean more losses during turn-off rather than the I_{RMS}^2 x $R_{DS(ON)}$ losses.
3. Charge and discharge of the gate capacitance is the third component of switching losses, fCV^2. Again, Supertex's low threshold MOSFET is an advantage due to the low threshold and low gate capacitance. Reducing the switching frequency can also reduce losses, but can increase the magnetic losses (described later).

Current Loop / Current Limit

Figure 4 details the current control loop of the HV9605C. Resistor R_7 converts the linearly increasing current ramp in T_1's primary winding into a voltage ramp. The low pass filter formed by R_6 and C_3 filters out the high frequency spikes generated by the switching action of Q_1. The high-speed modulator comparator in the HV9605C compares the current ramp with an error voltage (the feedback signal) and shuts off Q_1 when the current equals the error voltage. This is the "inner" control loop.

A current limit comparator in the HV9605C IC limits the peak current to a fixed maximum value in case of a short on the output. When the voltage across the current sense resistor R_7 reaches a nominal peak value of 0.7V, the current limit comparator will trip and turn Q_1 off.

Reducing the sense resistor value would also reduce power loss, I_{RMS}^2 x R_{SENSE}. However, it would affect the performance of the PWM regulation in two ways. First, if the sense resistor is low, then the trip level of the modulator comparator is low. If this falls below the sensitivity of

CURRENT SENSE CIRCUITRY

Under a high input voltage and low load condition, a high voltage spike could occur at the source of Q_1 due to the high drive capability of the HV9605C. This voltage spike could trip the over current sense function of the HV9605C. Two methods are employed to help prevent false triggering oft the over current protection circuitry: 1) gate resistor, and 2) RC filtering.

A gate resistor, R_5, is used to slowly turn on Q_1. This reduces the sudden current charge of the Q_1 gate which is coupled to the source through the C_{GS} parasitic capacitance. Thus generating a voltage spike on the sense resistor, R_7. A diode, D_4, is provided to allow Q_1 to turn off quickly and reduce power loss in Q_1 during the turn-off cycle.

An RC low-pass filter, R_6 and C_3, connected between Q_1 source and the CS pin of U_1 help reduce any remaining voltage spikes that would be seen during the turn on cycle of Q_1. The RC time constant needs to be high enough to suppress any spikes below the over-current threshold, 0.7V, but must be small enough as to not distort the current sense waveform to affect the control loop.

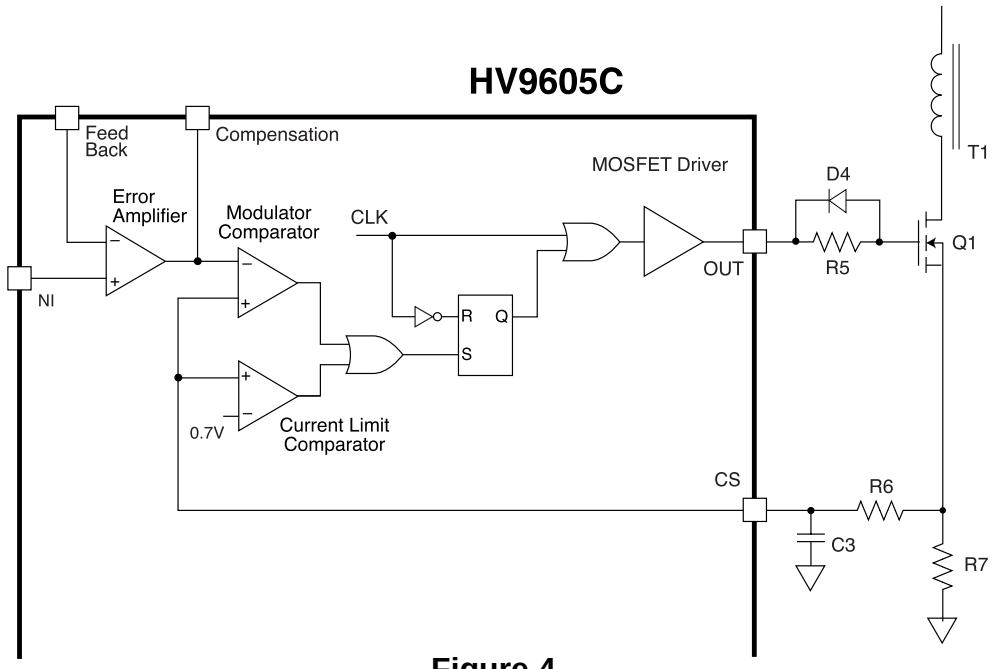

Figure 4

the modulator comparator, the supply could become unstable. Secondly, the turn-on spike, due to turning on the MOSFET, could also falsely trip either of the modulator or current limit comparator. This too, would result in unstable power supply operation.

Transformer

When Q_1 impresses the input voltage across T_1's primary, it causes the primary current to increase linearly with time. Two secondary windings are used to generate the necessary voltages to generate the 5V and 40V outputs to power both the HV9605C and typical ISDN circuits. Transformer design can be critical to efficiency due to the magnetic and winding losses associated.

Magnetic losses

When designing the transformer, the magnetics can make a significant effect on the efficiency. It is required to be aware of the maximum induced flux density, oscillation frequency, core volume, core area, and core material. Core loss is usually provided as a graph. A typical graph shows, for a particular material, flux density on the X-axis on a logarithmic scale, core loss per volume on a logarithmic scale, and operation frequency as a diagonal on a logarithmic scale. Details of specifically how these affect the magnetic loss is beyond the scope of this application note.

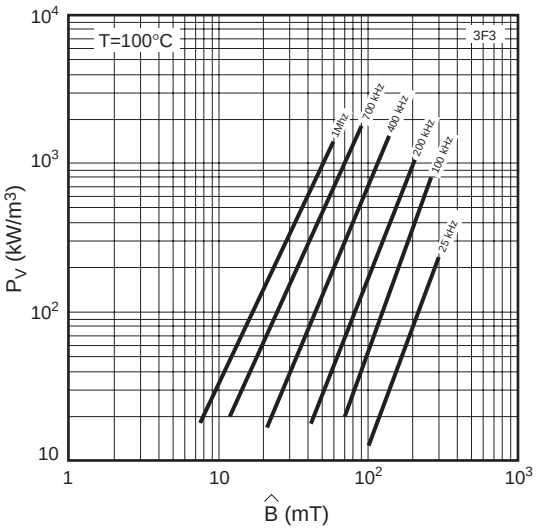

Figure 5

Winding losses

Winding losses are a function of the input and output current, and the size of the wire used. Increasing the wire size would reduce the losses linearly, $P_{CU} = I_{RMS}^2 \times R_{WIRE}$. However, a drawback to increasing the wire size could be the capability of fitting all of the windings on the transformer bobbin. This could result in a larger core and more core loss.

Output Rectifier and Filter

When Q_1 turns off, the energy stored in T_1 causes current to flow in the secondary windings. Diodes, D_2, D_3 and D_5, and capacitors, C_5, C_6 and C_9, integrate the currents from the transformer and provide output filtering.

The 5V output is regulated by the feedback control loop. The HV9605C supply voltage, V_{DD}, is regulated based on the 5V output regulation. The 40V output is controlled by the turn ratio between the 5V winding and 40V winding.

Output rectifier losses

When selecting the output rectifier diodes, it is imperative to use schottky diodes to minimize the forward voltage loss, $I_{OUT} \times V_F$. This could easily be a factor of two or more when using regular diodes with forward voltage drops exceeding two to three times the drop for a schottky diode.

In addition, selection of an ultra fast diode would reduce the rectifier losses by reducing the losses during the diode's turn-off transition.

Output capacitor losses

The output rectifier loss is typically expressed as a series resistance loss, $I_{OUT}^2 \times ESR$. Using high quality electrolytic capacitors and paralleling capacitors can significantly reduce the series resistance. And thus reduce the capacitor losses. The drawbacks to this would be higher cost components and more board space.

Feedback Control Loop

The 5V output is regulated using a resistor divider string, R_8 and R_9, to generate a 1.25V feedback voltage. The components C_7, R_{10}, and R_{11} provide compensation for the power supply regulation loop. The compensation components are selected to provide sufficient DC and AC gain to keep the regulation stable during load variations.

Start/Stop Accessory Circuit

The HV9605C contains an integrated start/stop circuitry. This allows the designer to program a starting voltage threshold and a stop threshold to keep the PWM converter from oscillating on and off. This condition can exist where there is a long feed line to the power supply, and the input to the supply can droop as the PWM converter starts. The circuit shown in Figure 5 is a simplified diagram of this start/stop circuit.

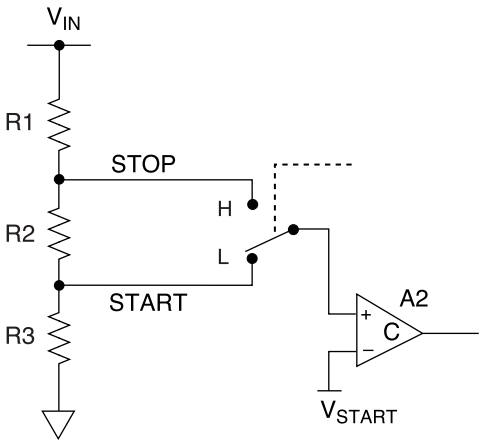

Figure 6

The selection of the three resistors is based on several equations.

$$V_{IN(START)} = V_{START}\frac{(R_1 + R_2 + R_3)}{R_3}$$

$$V_{IN(STOP)} = V_{START}\frac{(R_1 + R_2 + R3)}{(R_2 + R_3)}$$

$$I_{LEAKAGE} = \frac{V_{IN(START)}}{(R_1 + R_2 + R_3)}$$

$$V_{CLAMP} > V_{IN(START)}\frac{(R_2 + R_3)}{(R_1 + R_2 + R_3)}$$

Where,

R_1, R_2, R_3 are external resistors

$V_{IN(START)}$ is the input voltage, V_{IN}, for the converter to start

$V_{IN(STOP)}$ is the input voltage, V_{IN}, for the converter to stop

V_{START} is the trip threshold, 7.3V nominal on the inverting input of the comparator

$I_{LEAKAGE}$ is the maximum leakage current in the off condition

V_{CLAMP} is the internal input clamping voltage, 15V.

Status Output

The STATUS output is an N-channel open drain pull-down with a 10µA constant current pull-up to V_{DD}. An external capacitor, C_4, to ground is typically connected to the status pin. The Status output will remain low until the following three conditions are met: 1) The input voltage is within its programmed start/stop voltage, 2) The device is operating from the auxiliary winding, and 3) The internal error amplifier's output is not saturated to its upper limit. Once all these conditions are satisfied, the 10µA constant current source will start charging the external capacitor to V_{DD}. The charge time can be determined by the following equation.

$$t_{CHARGE} = C_4\frac{V_{DD}}{10\mu A}$$

The circuit in Figure 1 uses a 10nF external capacitor for a charge time of 5.0ms. When the STATUS pin is at V_{DD}, it indicates that normal operation has been reached. This can be used to control the reset of a microprocessor.

Conclusions

When the losses in a low wattage power supply seems high, start evaluating the specifications of the components used. Table I shows a summation of the losses discussed above and the theoretical efficiency. The actual efficiency will be slightly lower due to other component loss and switching losses not accounted for in the calculation.

Design Support

Supertex offers a variety of support for designing a power supply using the HV9605C. This includes application notes, spreadsheets, and personal support.

Application notes:

AN-H13: *Designing High-Performance Flyback Converters with the HV9110 and HV9120*

AN-H21: *Calculating Power Dissipation and Supply Current in HV91 Series Parts*

AN-H23: *Avoiding Turn-on Oscillations in HV91 Family PWM ICs*

AN-H24: *Expected Voltages and Waveforms from an HV9120-Controlled Flyback Converter*

Technical Support:

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Table I. *Theoretical losses for a 1W output, 48V input HV9605C power supply.*

Loss component	***Calculation***	***Losses, mW***
Start up circuit	48V * 20μA	0.96
HV9605C operating supply	5V * 0.9mA max	4.50
Magnetics loss 2616 core, 3F3 material, 700 Gauss, 33kHz	$3.53cm^3$ * $0.7mW/cm^3$	2.47
Winding losses		
Primary	$22.5mA^2$ * 1.5Ω	0.76
5V	$100mA^2$ * 0.8Ω	8.00
40V	$12.5mA^2$ * 5.8Ω	0.91
Switching losses		
DC losses, $R_{DS(ON)}$	$22.5mA^2$ * 6Ω	3.00
Switching, fCV^2	33kHz * 125pF * $(5V)^2$	0.10
Output rectifiers		
5V	100mA * 0.41V	41.00
40V	12.5mA * 1.2V	15.00
Output capacitors		
5V	$100mA^2$ * 4Ω	40.00
40V	$12.5mA^2$ * 2Ω	0.31
	TOTAL LOSSES	117.01
	Efficiency	90%

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